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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/837,022	04/18/2001	Hiroshi Kimura	TKA0029	7517

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EXAMINER
MITCHELL, JAMES M

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 02/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/837,022	KIMURA, HIROSHI	
	Examiner	Art Unit	
	James Mitchell	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 December 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 4-9* is/are pending in the application.

4a) Of the above claim(s) *1,4 and 9* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election

Claims 1, 4 and 9 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in Paper No. 8. Applicant indicates that it is unaware of a semiconductor device structure that does not include a removing step. However the removing step referenced was in context of the method, requiring "removing said metallic substrate," which applicant later correctly asserted in the following paragraph. Since applicant's device does not disclose a metallic substrate, any reference to a preliminary step of removing the substrate that is not apart of the final product is deemed unpersuasive. The restriction is appropriate under chapter 800 of the M.P.E.P and thus made final.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi (US 6,166,430) in combination with Glenn and Jung et al.

Yamaguchi (Fig 9a-e) discloses a method of manufacturing a semiconductor device comprising steps of forming an electrodeposition frame on a flexible substrate (28), said electrodeposition frame having first metallic layers (24) and second metallic

layers (22) for external extension being patterned, wherein the first metallic layers are thicker than said second metallic layers, contiguously mounting a semiconductor with electrode pads (23a) thereon on said first metallic layers, wire bonding (25) the electrode pads to said second metallic layers, resin-sealing (26) said semiconductor element mounted on said electrodeposition frame using the substrate as a lower die, removing said substrate (Fig 9e) to provide a resin sealing body (Fig 9f); cutting said second metallic layers (Col. 11, Lines 62-63).

Yamaguchi does not appear to disclose a plurality of semiconductor elements, cutting a resin sealing body into individual semiconductor devices, a metallic flexible substrate, after cutting depositing metallic layers for electrodes to the second metallic layers exposed from a rear surface of said resin sealing body or the first and second metallic layers between about 20 to 35 micrometers.

Glenn (Fig 1; Col. 6, Lines 5-7) utilizes a method of manufacturing semiconductor devices comprising cutting a resin sealing body of a plurality of semiconductor elements to form into individual semiconductor devices and depositing metallic layers for electrodes to the second metallic layers (34; Col. 3, Lines 14-17) exposed from a rear surface of said resin sealing body.

It would have been obvious to one of ordinary skill in the art to one of ordinary skill in the art to utilize the packaging method for a plurality of semiconductor devices for mass fabrication, to cut the resin in order to separate the package into individual packages and to provide metallic layers for electrodes to the second metallic layers

exposed from a rear surface of said resin sealing body in order to connect the package to external circuitry as taught by Glenn (Col.5, Lines 65-67).

Furthermore, it would have been obvious to one of ordinary skill of the art to form a plurality of semiconductor devices, since it has been held that mere duplication of the working parts of a device involves only routine skill in the art. *In re Japiske*, 86 USPQ 70 (CCPA 1950).

As for depositing metallic layers for electrodes after said cutting and in said step of cutting said resin cut along center line of the second metallic layers, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed sequence because applicant has not disclosed that the limitation is for a particular unobvious purpose, produces an unexpected result, or is otherwise critical. Moreover, it is well established that, in a well known process, the order of performing process steps is prima facie obvious in the absence of new or unexpected results. Ex parte Rubin 128 USPQ (PO BdPatApp 1959).

Jung utilizes an inherently flexible metallic substrate (260) to enable a package body to be formed over a semiconductor chip (Fig 9-11; Col. 21, Lines 24-26). It would have been obvious to one of ordinary skill in the art to form Yamaguchi's substrate as a metallic substrate, since both plastic and metallic bases are well known in the art as temporary bases used to form a package body over a semiconductor chip.

Furthermore, it would have been obvious to one of ordinary skill in the at the time the invention was made to use a metallic substrate as an alternate temporary substrate,

since it has been held that to be within the general skill of a worker in the art to select known material on the basis of its suitability for intended use as a matter o f obvious design choice. *In re Leshin*, 125 USPQ 416 (1960).

Claims 5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jung et al. in combination with Glenn.

Jung (Fig 6, 9, 10, 11) discloses a method of manufacturing a semiconductor device comprising steps of forming an electrodeposition frame on a flexible flat metallic substrate (260), said electrodeposition frame having first metallic layers and (250,240, 232; beneath chip 210) and second metallic layers for external extension being patterned, wherein the first metallic layers has an extent from one surface to its opposite and therefore is thicker than said second metallic layers ("connection pad", 230 of metal layer 270), contiguously mounting a semiconductor elements (210) each with electrode pads thereon (210a) on said first metallic layers, wire bonding (212) the electrode pads to said second metallic layers, resin-sealing (220) said semiconductor element mounted no said electrodeposition frame, removing said metallic substrate (Column 4, Lines 25-27) to provide resin sealing body (Fig 11) wherein rear surface of the first and second metallic layers are flush with a bottom of said resin package, and wherein the second metallic layer is individually exposed from a bottom of said resin package (Paragraph 0021, Lines 9-10).

Jung does not appear to disclose a plurality of semiconductor elements, cutting a resin sealing body into individual semiconductor devices, after cutting depositing metallic layers for electrodes to the second metallic layers exposed from a rear surface

of said resin sealing body or the first and second metallic layers between about 20 to 35 micrometers.

Glenn (Fig 1; Col. 6, Lines 5-7) utilizes a method of manufacturing semiconductor devices comprising cutting a resin sealing body of a plurality of semiconductor elements to form into individual semiconductor devices and depositing metallic layers for electrodes to the second metallic layers (34; Col. 3, Lines 14-17) exposed from a rear surface of said resin sealing body.

It would have been obvious to one of ordinary skill in the art to utilize the packaging method of Jung for mass fabrication, to cut the resin in order to separate the package into individual packages and to provide metallic layers for electrodes to the second metallic layers exposed from a rear surface of said resin sealing body in order to connect the package to external circuitry as taught by Glenn (Col.5, Lines 65-67).

Furthermore, it would have been obvious to one of ordinary skill of the art to form a plurality of semiconductor devices, since it has been held that mere duplication of the working parts of a device involves only routine skill in the art. *In re Japiske*, 86 USPQ 70 (CCPA 1950).

Lastly, depositing metallic layers for electrodes after said cutting and in said step of cutting said resin cut along center line of the second metallic layers, would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed sequence because applicant has not disclosed that the limitation is for a particular unobvious purpose, produces an unexpected result, or is otherwise critical.

Moreover, it is well established that, in a well known process, the order of performing process steps is prima facie obvious in the absence of new or unexpected results. Ex parte Rubin 128 USPQ (PO BdPatApp 1959).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Mitchell whose telephone number is (703) 305-0244. The examiner can normally be reached on M-F 10:30-8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on (703) 305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 305-3230 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

jmm
January 27, 2003

John B. Vigushin
EXR. JOHN B. VIGUSHIN
GAU 2827